Processes Limiting the Performance of InAs/GaSb Superlattice Mid-Infrared PIN Mesa Photodiodes

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ABSTRACT

In this study, we examine processes limiting the performance of 4 micron superlattice pin photodiodes for different temperature and mesa size regimes. We show that the performance of large mesa photodiodes at low temperature is most severely limited by a trap-assisted tunneling leakage current (x300), while small mesa sizes are additionally limited by perimeter leakage (x20). At room temperature, large mesa photodiodes are limited by the diffusion current, and small mesa photodiodes are further limited by the perimeter leakage (x100). To reduce or eliminate the impact of perimeter leakage, we have tried passivating the mesa sidewalls with SiN, an approach that was only minimally successful. We have also laid the groundwork for another approach to elimination of perimeter leakage currents, namely, elimination of the sidewalls altogether through planar processing techniques. Planar processing schemes require the deposition of a thick, wide bandgap semiconductor or "window layer" on top of the homojunction. We compare the performance of two otherwise identical InAs/GaSb superlattice homojunction detectors, except one with a GaSb window layer, and one without. We show that inclusion of the thick GaSb window layer does not degrade detector performance.

Keywords: InAs/GaSb superlattice, photodiode detector, MBE growth, wet etching, perimeter leakage, trap-assisted tunneling leakage, planar processing

1. INTRODUCTION

The detection of mid- and long-wavelength infrared (MWIR, LWIR) radiation is of growing importance in a number of industries and encompasses military, industrial, and biomedical applications. In recent years, research on a Type II superlattice (SL) structure consisting of alternating thin layers of InAs and InGaSb alloys has shown the potential for high-sensitivity, high-temperature operation that can outperform existing LWIR detectors available today. The binary/binary InAs/GaSb SL system, first proposed for IR detection in 1977, [1] has a staggered Type II band alignment in which the InAs conduction band is lower than the GaSb valence band. Quantum confinement in SL layers of appropriate thickness allows for the tuning of the SL bandgap. In 1987, Smith and Mailhiot proposed the closely related binary/ternary SL, InAs/$In_xGa_{1-x}Sb$, in which strain effects, in addition to quantum confinement, allow for greater design flexibility and improved device characteristics.[2] Bandgaps between 0 and 400 meV can be achieved, leading to an enormous range of detector cutoff wavelengths. Moreover, the benefits of this material system extend well beyond the tuning of the bandgap energy: in fact, the entire SL band structure can be "engineered" to create desirable device properties. By an appropriate variation of layer thickness and composition, one can derive numerous structures that have the same bandgap but different band structure characteristics. For instance, for a given bandgap, it is possible to tailor the light-hole and heavy-hole band separation to suppress Auger recombination with a consequent increase in carrier lifetime.[3,4] It is also possible to achieve designs with more optimal layer thicknesses that provide better absorption properties[2] (by using sufficiently thin layers) while avoiding the problems of interface variability (encountered when layers are too thin).

With regard to the wafer-level processing and device design approaches applied to InAs/InGaSb SL detectors, there is considerable opportunity to improve on the work done to date. Recently, there has been recognition that perimeter leakage currents can limit the performance of MWIR and LWIR InAs/InGaSb SL mesa diode detectors.[5] In our study, we map out the impact of perimeter leakage on detector performance as a function of mesa size and temperature of

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operation. We show perimeter leakage strongly limits the performance of small mesa photodiodes, important for dense focal plane arrays with small detector pixels. We also show the performance of cooled photodiodes to be strongly limited by trap assisted tunneling.

We pursue a strategy to passivate the sidewalls by coating them with a SiN dielectric. As with other recent passivation attempts, our dielectric passivation approach met with only limited success. The current state of development of InAs/InGaSb SL detectors has parallels two decades ago with the first efforts to industrialize InP-based p-i-n photodiodes with lattice-matched InGaAs absorption regions: mesa-geometry devices were found to be very difficult to passivate, and a key breakthrough in device commercialization was the migration to planar-passivated device geometries. We believe that a comparable approach can be very fruitful in the context of the InAs/InGaSb SL detectors. Planar processing approaches typically require thick, wide bandgap semiconductor window layers. To lay the groundwork for a planar processing approach, we compare the performance of two identical InAs/GaSb SL homojunction photodiodes, one with a thick GaSb window layer, and one without.

2. MBE GROWTH

All samples for this study were grown in a Veeco-Applied Epi 930 molecular beam epitaxial system equipped with valved crackers for the group V materials Sb and As, and dual filament SUMO cells for the group III materials In and Ga. Sb and As cracking zones were held at 1000 ºC and 900 ºC, respectively, yielding monomeric Sb and As_2. InAs/GaSb superlattices were grown on 2", p-type, (100)-oriented GaSb substrates 500 microns thick. Substrates were etched for 1 minute in concentrated HCl to thin the oxide layer along with pre- and post- degreasing steps, which we have found leads to improved post epi-growth surfaces, consistent with previous studies.[6] Substrates were first outgassed in the intro chamber for 2 hours at 175 ºC, 1 hour at 350 ºC (thermocouple temperature) in the buffer chamber, and then the oxide layer was thermally desorbed in the growth chamber under an Sb beam equivalent pressure (BEP) flux of 7×10^{-7} Torr. After the onset of desorption at about 495 ºC according to an optical pyrometer, the substrate was heated to 515 ºC for 10 minutes to ensure full removal of the oxide layer across the substrate. The optical pyrometer was calibrated with respect to a 1×3 to 1×5 reflection high energy electron diffraction (RHEED) pattern transition, which was observed to occur at 400 ºC under a monomeric Sb BEP flux of 7×10^{-7} Torr.

A 500 nm thick p-GaSb buffer layer was first grown on the p-GaSb substrate at 480ºC, according to the optical pyrometer. The substrate was cooled to 410 ºC during the last part of the buffer layer growth, which previous studies show gives optimal photoluminescence and minimal residual doping levels,[7] and then growth of the superlattice was begun. The GaSb layer was grown at a rate of 0.5 ml/sec with a V/III BEP flux ratio of about 6, while the InAs was grown at a rate of 0.174 ml/sec with a BEP V/III flux ratio of about 1. The InAs layer was grown slowly and as close to stoichiometric conditions as possible in order to minimize the As_2 BEP flux (1.2×10^{-7} Torr) and hence excess As in the chamber, which studies have shown tends to contaminate the GaSb layer, and in high enough levels grade the superlattice and roughen the growth.[8] Further, during the growth of the GaSb layer, the As valve was closed in addition to the shutter to prevent As_2 from getting around the shutter. During growth of the InAs layer, the Sb shutter but not the valve was closed. The normal interfaces (GaSb on InAs) were forced to be InSb-like using a controlled Sb soak between layers (5 sec, 1.0×10^{-6} Torr BEP Sb). The inverted interfaces (InAs on GaSb) were forced to be GaAs-like by using a controlled As_2 soak between layers (15 sec. 1.2×10^{-7} Torr BEP As_2).[9,10,11]

For this study, two nominally four micron (310 meV) InAs/GaSb (8 ml/16 ml) superlattice pin homojunction structures (90, 40, 60 periods for the p, i, and n regions, respectively) were grown. Structure ia1460 was capped with 500 nm of n-GaSb, a wide bandgap window layer, while ia1464 contained no window layer. Both samples were capped with a thin, heavily doped n-InAs contact layer. After growth, the superlattice structure was characterized by simulating a high resolution x-ray diffraction (HRXRD) measurement of the structure using BEDERADS commercial software. Measurement and simulation of the structures for this study are shown in Fig. 1. Parameters for the simulated fits are summarized in Table 1. Both samples showed excellent structural quality, particularly ia1464, as indicated by the good fit between the simulated and measured HRXRD rocking curves.

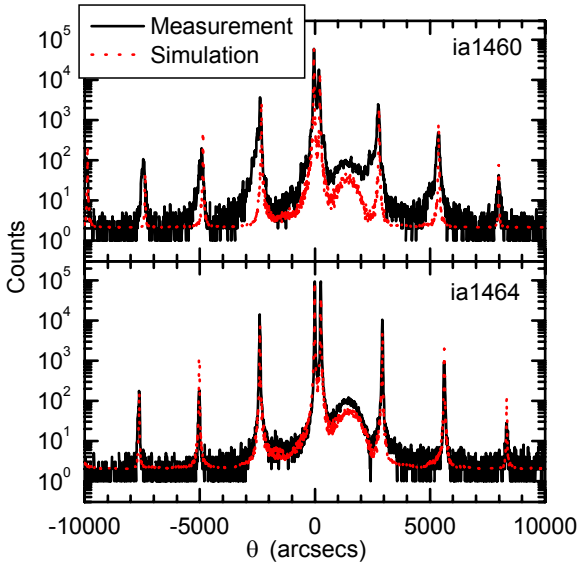

Fig. 1 Measured and simulated high resolution x-ray diffraction (HRXRD) rocking curve of the two detector structures grown for this study. Parameters used in the simulation are summarized in Table I. The good agreement between measured and simulated rocking curves shows excellent structural quality, particularly for ia1464.

InAs 19.5 nm (n=4e18)	
GaSb 511 nm (n=1e18)	
GaSb 15.3 MLs	×60 (n=3E17)
InSb 1.0 MLs	
InAs 6. 8 MLs	
GaAs 0.5 MLs	
GaSb 15.3 MLs	×40 (undoped)
InSb 1.0 MLs	
InAs 6.8 MLs	
GaAs 0.5 MLs	
GaSb 15.3 MLs	×90 (p=2E17)
InSb 1.0 MLs	
InAs 6.8 MLs	
GaAs 0.5 MLs	
GaSb 500nm (p=2E18)	
2” p-GaSb Substrate	

IA1460 InAs/GaSb (8MLs/16MLs) 4 μm SL pin detector, alternating interface type, with GaSb window

InAs 19.5 nm (n=2e18)	
GaSb 14.5MLs	×60 (n=3E17)
InSb 1.0 MLs	
InAs 6.8 MLs	
GaAs 0.5 MLs	
GaSb 14.5 MLs	×40 (undoped)
InSb 1.0 MLs	
InAs 6.8MLs	
GaAs 0.5 MLs	
GaSb 14.5MLs	×90 (p=2E17)
InSb 1.0 MLs	
InAs 6.8 MLs	
GaAs 0.5 MLs	
GaSb 500nm (p=2E18)	
2” p-GaSb Substrate	

IA1464 InAs/GaSb (8MLs/16MLs) 4 μm SL pin detector, alternating interface type, no GaSb window

Table I Summary of parameters used in the simulation of the HRXRD measurement of the detector structures in Fig. 1.

The bandgap of the superlattice was checked with a low temperature (77 K) photoluminescence measurement. The photoluminescence peak in Fig. 2 gives a measured bandgap of about 3.8 microns (326 meV). The measurement was performed prior to the growth of the detector structures on an identically grown superlattice sample (ia1455).

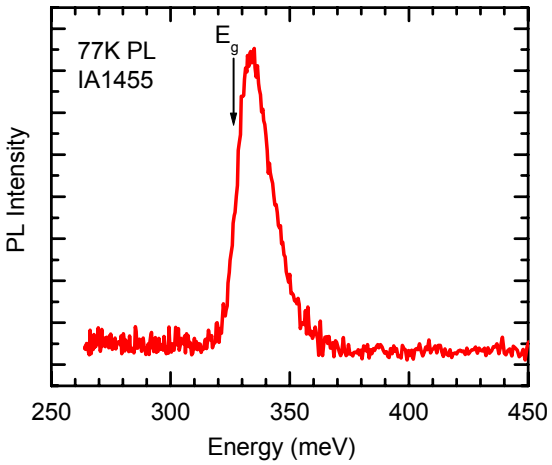

Fig. 2 Low temperature (77K) photoluminescence of a superlattice structure (ia1455) grown prior to the detector structures. The superlattice was grown in the same way as the detector superlattice. The measured energy gap is about 3.8 microns (326 meV).

3. DEVICE PROCESSING

A TiPtAu p-metal stack with layer thicknesses of Ti(500Å)/Pt(600Å)/Au(1500Å) was deposited using e-beam deposition. After liftoff and photolithography with a positive photoresist, the samples were etched to form mesas. In our process, the optimized etch chemistry was [Citric Acid : H_3PO_4 : H_2O_2] that resulted in nearly vertical sidewall profile to a depth of about 2 μm, just beyond the depth of the window layer and superlattice. The etch depth for the structures with and without GaSb window (IA1460, IA1464) was measured by profilometry to be 2.85 and 1.9 μm. We observed a wafer-dependent variation in the impact of mesa etching on surface morphology: while the etched surface of IA1460 was somewhat rougher than the surface prior to etching, the IA1464 roughness was approximately the same before and after etching.

After mesa etching, back side contact metals were e-beam deposited to obtain a stack composition of Ti(500Å)/Pt(600Å)/Au(2000Å). The samples then were subjected to a rapid thermal anneal at 375 °C for 45 s to alloy the contacts. After alloying the contacts, the samples were cleaved into two halves, and the first half of each sample was ready for testing of non-passivated devices. The surfaces of the second halves were passivated by depositing a blanket coating of 3500 Å of SiN. Electrical access to the contacts was provided by removing the SiN layer by reactive ion etching where it overlapped the contact pads.

4. DEVICE CHARACTERIZATION

The wafer was chipped in to 3 × 2 mm test samples. Each test sample consisted of a set of devices with circular and ring shapes that provided various device perimeters and areas. The biggest and smallest devices in the test set had radiuses of 240 and 40 μm respectively. Test samples were soldered onto a convenient multi-lead ceramic chip carrier. The individual devices were wire-bonded to the leads of the chip carrier, which in its turn was bolted onto the copper finger in the liquid nitrogen-cooled cryostat for the characterization of detectors between 80K and 320 K. The measurements at low temperature were performed in the cryostat at pressure of about 15–20 torr, sufficiently low to prevent water condensation.

5. RESULTS AND DISCUSSION

P-i-n detectors operate by generation of a current of electrons and holes from the absorption of incident light within a diffusion length of the the depletion region. From the depletion region, electrons and holes are accelerated to the n and p

regions, respectively, where they are collected by the metal contacts. In the following discussion, both the detectors are analyzed in terms of the zero bias dynamic resistance, defined as $(R_0=dI/dV)^{-1}{}_{V=0}$, —mesa area (A) product R_0A. Together with spectral responsivity R_λ, defined as the Amps of current generated by the detector at zero bias voltage per Watt of incident light, these two important figures of merit characterize the D* of the detector, which is a measure of the S/N of the detector per unit incident radiation: $D^*(\lambda) = R_\lambda(R_0A/4k_BT)^{1/2}$, where k_B is the Boltzman constant and T is the temperature. The analysis here is mainly focused on R_0A, which is primarily impacted by leakage currents at the perimeter and surface of the mesa diode.

5.1 Currents limiting R_0A versus temperture

Current-voltage (J-V) curves were measured for variable size mesas of both detector structures IA1460 and IA464 as a function of temperature. Figure 3 shows the representative variation in R_0A on semilog scale as a function of 1000/T for mesas with three different radii: r=60, 120, and 240 μms. The data shows that initially, as the sample is cooled down from above room temperature 337 K, the R_0A increases exponentially. As lower temperatures are attained, however, there is "roll-off" in R_0A. For all temperatures, there is a general improvement in R_0A going to larger diodes, indicating that perimeter leakage degrades the performance of the smaller mesa photodiodes.

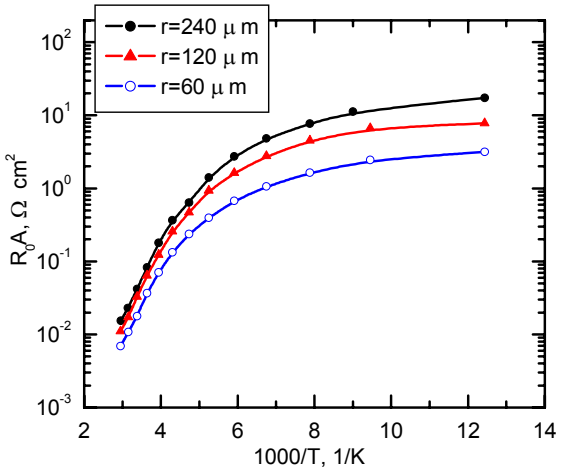

Fig. 3 Dynamic resistance—area product R_0A versus 1000/T for mesas with three different radii r=60, 120, and 240 μm processed in the same run on ia1460. The R_0A increases sharply as the temperature is initially reduced, but then "rolls off" at lower temperature. For all temperatures, there is a general improvement in R_0A going to larger diodes, indicating that perimeter leakage degrades the smaller mesa diodes.

To understand the origin of the temperature dependence of R_0A, we modeled the room and low temperature J-V curves using the standard generation-recombination (G-R)-diffusion-Zener tunneling model,[12] which is reproduced here for reference (SI units):

$$J_{diff} = n_i^2(T)\sqrt{ek_BT}\left(\frac{1}{N_A}\sqrt{\frac{\mu_e}{\tau_e}}+\frac{1}{N_D}\sqrt{\frac{\mu_h}{\tau_h}}\right)\left(\exp(eV/k_BT)-1\right) \tag{1}$$

$$J_{GR} = \frac{-en_i(T)d(V)}{\tau_{GR}}\frac{\sinh(-eV/2k_BT)}{e(V_{bi}-V)/2k_BT}f(b) \tag{2}$$

$$J_T = \frac{e^3F(V)V}{4\pi^2\hbar^2}\sqrt{\frac{2m_T}{E_g}}\exp\left(-\frac{4\sqrt{2m_TE_g^3}}{3e\hbar F(V)}\right) \tag{3}$$

where $n_i(T)$ is the temperature-dependent intrinsic carrier concentration, e is the electron charge, k_B is Boltzman's constant, T is temperature, N_A and N_D are the acceptor and donor densities in the p and n regions, respectively; μ_e, τ_e, and μ_h, τ_h are the mobility and lifetime of electrons and holes, respectively; V is the bias voltage and V_{bi} the built in potential; τ_{GR} is the generation recombination lifetime; m_T is the tunneling effective mass; E_g is the bandgap, $\hbar$ is Planck's constant; d(V) is the depletion width; F(V) is the electric field in the depletion region, and

$$f(b) = \int_0^\infty \frac{du}{u^2 + 2bu + 1}, \; b = \exp\left(-\frac{eV}{2k_B T}\right). \tag{4}$$

Due to background p-doping of the i-layer, the homojunction is a p+pn+ structure, and so the width of the depletion layer is not the width of the i-region, as would be the case of a true pin homojunction, but that of a p/n+ homojunction:

$$d(V) = \left[\frac{(N_D / N_B)}{N_D + N_B}\left[\frac{e(V_{bi} - V)}{2\pi e}\right]\right]^{1/2} \tag{5}$$

Where N_B is the background (p) doping level.

We also included in our analysis a trap-assisted tunneling process, and expressed it in the form of an areal leakage by averaging the traps along the perimeter and in the junction over the volume of the junction:[12,13]

$$J_{trap} = cV \exp(-(E_g - E_t)/k_B T) \exp\left(-\frac{4\sqrt{2m_T (E_g - E_t)^3}}{3e\hbar F(V)}\right), \; c \equiv \frac{e^2 m_T M^2 N_0}{8\pi\hbar^3} \tag{6}$$

where N_0 is the spatially averaged trap density, and E_t is the trap depth with respect to the valence band edge, and m_T is the tunneling effective mass, N_0 is the trap density, and M is a transition matrix element associated with the trap.

Using the above model, we simulated the J-V curves for the 240 micron mesa of ia1460 at 293K and 77K, shown in Fig. 4 in comparison to experimental data. The parameters used for the model were: $\tau_e = \tau_h = 2\times10^{-9}$ s, $\tau_{GR} = 1.1\times10^{-9}$ s, $\mu_e = 1000$ cm^2/Vs, $\mu_h = 100$ cm^2/Vs, $N_A = 2\times10^{17}$ cm^{-3}, $N_D = 3\times10^{17}$ cm^{-3}, $N_B = 1\times10^{15}$ cm^{-3}, $V_{bi} = E_g/e$, $E_g = 310$ meV, $E_t = E_g - 25$ meV, $m_T = m_e = 0.039m_0$, $m_h = 0.4m_0$ (m_0 the free electron mass), $\varepsilon = 3.6^2\varepsilon_0$ (ε_0 the permittivity of free space), and $c = 24(\Omega\text{-cm}^2)^{-1}$.

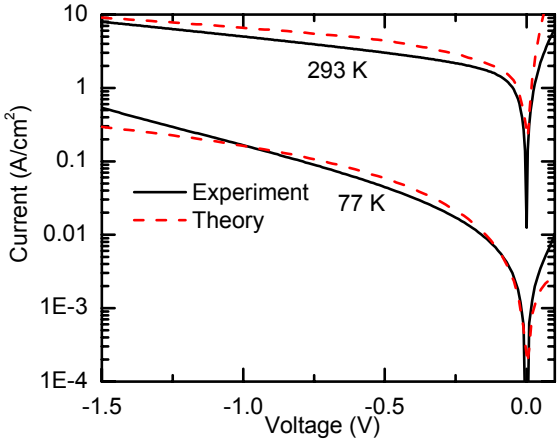

Fig. 4 Good qualitative agreement is seen in a comparison of a theoretical simulation and experimental measurement of the J-V characteristics at 77K and 293K of a 240 μm mesa diode processed on the ia1460 sample.

Figure 4 shows good qualitative agreement between the theoretical simulation and the experimental measurement. Looking first at the 293 K data, a breakdown of the different contributions to the total simulated current is shown in Fig. 5. Figure 5 shows that over most negative bias voltages, the total current through the diode is dominated by the generation-recombination current. Note the shape of the generation-recombination current with increasing negative

bias: first it increases fairly sharply, then increases only gently. This is in contrast to the diffusion current, which after an initial very sharp rise, saturates with increasing negative bias; and in contrast to the trap-assisted tunneling current, which increases more slowly initially and more quickly with increasing negative bias compared to the generation recombination current. In fact, its shape looks very like the J-V curve shown in Fig. 4 recorded at 77 K. A plot similar to Fig. 5 except for the 77 K case confirms that at low temperature, both the generation-recombination current and the diffusion current are orders of magnitude smaller than the trap-assisted tunneling current for bias voltages from 0 to -1.5 V. Zener tunneling current is orders of magnitude smaller than all other contributions at both 293 K (so small it does not appear in Fig.5) and 77K.

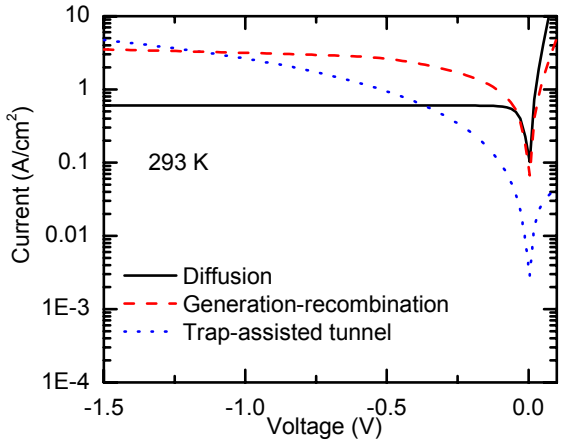

Fig. 5 Breakdown of the contributions to total current through the mesa diode at 293K corresponding to the simulated J-V curve in Fig. 4. At room temperature, the generation-recombination current dominates for the negative bias voltages shown here. The tunnel current is too small to appear in the plot.

Of course R_0A, the principal electrical figure of merit for a detector sensitivity, depends on the inverse differential current and not on total current:

$$R_0 A = \frac{1}{\sum_i dJ_i / dV|_{V=0}} \quad \text{, i = diffusion, generation-recombination, trap-assisted tunnel, and tunnel.} \qquad (7)$$

Now that parameters for the current contributions have been obtained from modeling the J-V curves, the contributions to R_0A as a function of temperature can be plotted as in Fig. 6. We see that the largest contributions to the differential current dJ/dV at room temperature is the differential diffusion current, and hence at room temperature the R_0A is diffusion limited (Eq. 7). As the temperature is decreased, the magnitude of the differential diffusion decreases sharply, and R_0A is then most strongly limited by the generation-recombination current. At lowest temperatures, it is the trap-assisted tunneling that most severly limits R_0A.

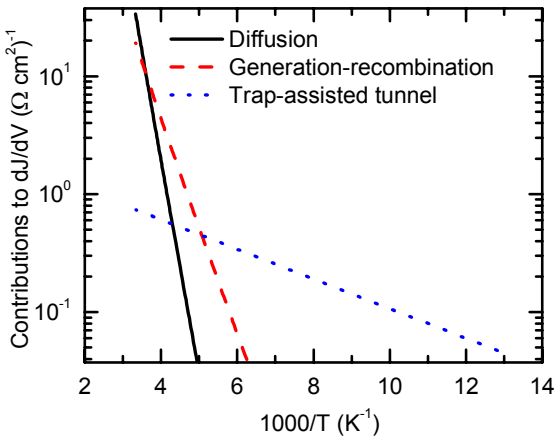

Fig. 6 Scaling of the contributions to the total zero-bias differential current dJ/dV, which is inverse to the dyanamic resistance-area product R_0A, as a function of 1000/T using the same parameters used to simulate the J-V curves in Fig. 4.

From Eqs.1-7 and the parameters obtained from Fig. 4, the zero bias dynamic resistance R_0A can be calculated, and is shown in Fig. 7 where it is compared to the measured R_0A, again for the 240 μm mesa on ia1460. The agreement between experiment and theory is very good. Note no fitting parameters have been used for the comparison of theory and experiment in Fig. 7; the same parameters used in the simulation of the J-V's in Fig. 4 are also used in the calculation of R_0A versus 1000/T in Fig. 7. Our analysis in Fig. 6 shows it is the trap-assisted tunneling that causes the roll-off in R_0A at low temperature. If we simply turn off the trap-assisted tunneling contribution to the current in the model, the low temperature R_0A improves by a factor of about 300, and is then limited by the differential generation-recombination current.

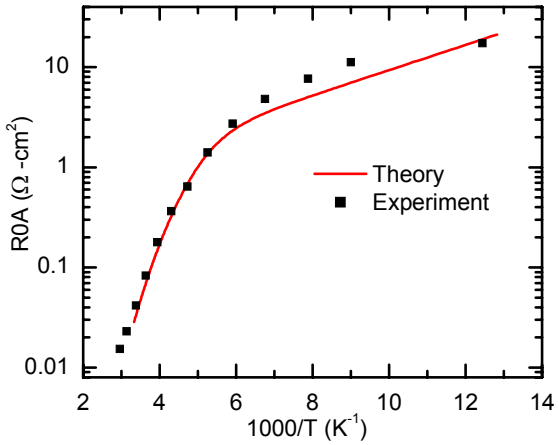

Fig. 7 Comparison of the temperature dependence of the experimentally measured R_0A of ia1460 r=240 μm radius mesa to theory using the same parameters as used to simulate the J-V curves in Fig. 4.

5.2 Impact of perimeter leakage currents on R_0A

An ambiguity of the above analysis is that the model for trap-assisted tunneling does not specify where the traps actually are, because it only includes a volumetric average density of the traps. For example, it is not clear if the traps are limited to the perimeter, or if they occur somewhere in the junction itself. To answer this question, we looked directly at the

degree to which perimeter leakage limits the mesa photodiode performance. Figure 8 shows a plot of $1/R_0A$ versus perimeter-to-area ratio at room temperature for ia1460 at 80K. It is evident that as mesas get smaller (larger perimeter-to-area ratio), R_0A decreases, indicating that perimeter leakage plays a role.

The linearity of $1/R_0A$ versus perimeter-to-area ratio can be understood on the basis of a simple physical picture, and used to separate out perimeter leakage effects for intrinsic junction performance. We can imagine the mesa diode as consisting of two resistors in parallel, a surface resistor R_{diode} and an edge resistor R_{edge}. Then the total diode resistance can be calculated:

$$\frac{1}{R_0 A} = \frac{1}{R_{diode} A} + \frac{1}{R_{edge} A}. \tag{8}$$

$R_{diode}A$ is independent of area, while R_{edge} should decrease with mesa radius as 1/r and hence $1/R_{edge}A$ should increase as 1/r, which is equal to one-half the perimeter-to-area ratio of circular mesas:

$$\frac{1}{R_0 A} = \frac{1}{R_{diode} A} + m\frac{2}{r} \tag{9}$$

where $m=(R_{edge}2\pi r)^{-1}$ is a constant. Eq. 9 is then the equation of a straight line with the maximum attainable R_0A one over the y-intercept in Fig. 8 (i.e. limit of infinite mesa radius). We find that the best value for the low-temperature R_0A in the limit of no perimeter leakage is 7 Ω-cm^2 (5-14 Ω-cm^2 using a least squares regression analysis). The maximum measured R_0A for our largest diodes at 80 K is 3 Ω-cm^2. Thus we can conclude that perimeter leakage does not significantly degrade the performance of the largest mesa diodes.

If perimeter leakage does not limit the performance of the largest diodes, then it follows that trap-dependent tunneling leakage, which severly limits low temperature performance (x300), as shown in Figs. 6-7, must occur in the junction, and not at the perimeter.

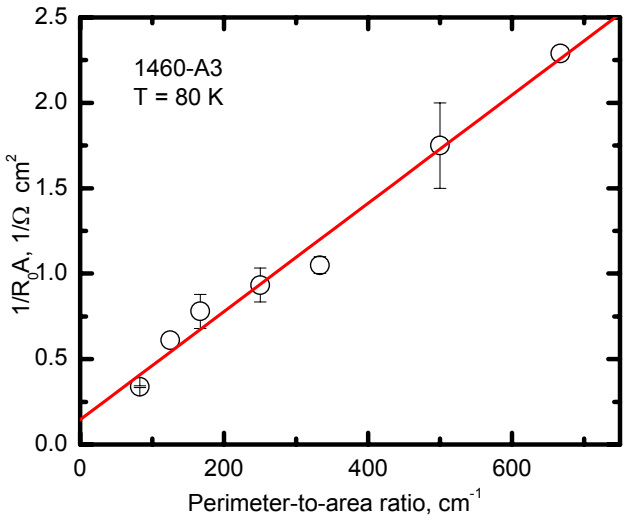

Fig. 8 Measured $1/R_0A$ of ia1460 versus perimeter-to-area ratio at 80 K (points), and least squares fit to the data (red).

The overall conclusions of our analysis of room and low temperature J-V's and R_0A are that at room temperature, R_0A in the largest mesas is limited predominantly by the diffusion and generation-recombination currents. The roll-off in R_0A at lower temperatures is due to trap-assisted tunneling that occurs in the junction. At low temperature, perimeter leakage does not substantially effect the largest mesa photodiodes, but reduces the R_0A of the smallest mesa photodiodes by a factor of about 20.

An implication of the above data and analysis to focal plane array detectors with densely packed pixels or even small single pixel detectors is that their sensitivity will be strongly limited by perimeter leakage currents. It motivates research into finding ways to minimize or even eliminate perimeter leakage current. One approach to minimizing perimeter leakage is through passivation of the sidewalls with a dielectric coating. As described in Sec. 3, we used SiN to passivate the sidewalls of mesa diodes fabricated from both samples ia1460 and ia1464. The results of passivated and unpassivated diodes are shown in Figs. 9 and 10.

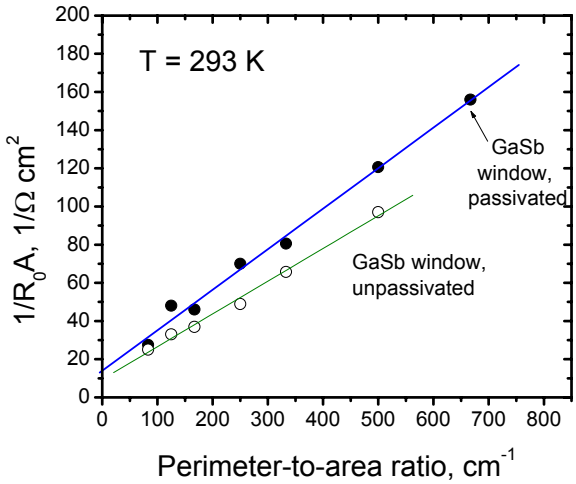

Fig. 9 **1**/R_0A vs. perimeter-to-area ratio for SiN passivated and unpassivated devices from ia1460, which has a GaSb window layer.

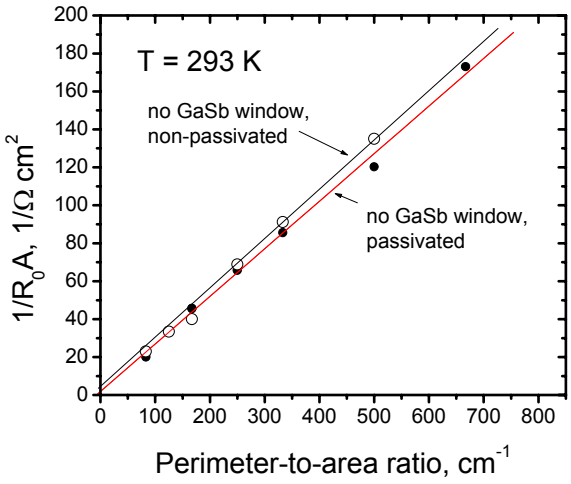

Fig.10 $1/R_0A$ vs. perimeter-to-area ration for SiN passivated and unpassivated devices from ia1464, which did not have a GaSb window layer.

Using the model of two parallel resistors, we separate out the intrinsic R_0A of the unpassivated mesa photodiodes in ia1464 (Fig. 10) to be 0.5 Ω-cm^2; the maximum measured R_0A to be 0.05 Ω-cm^2; and the minimum measured R_0A of 0.006 Ω-cm^2. At room temperature, we see that the R_0A of the smallest mesa photodiodes are limited by perimeter leakage by a factor of about 100. Looking in Fig. 10 at the R_0A of the mesa photodiodes in ia1464 with sidewalls passivated by SiN, we see that for all mesa sizes, there is only a small improvement in R_0A. For passivated compared to unpassivated mesa photodiodes in ia1460, shown in Fig. 9, the results flip-flop, and the unpassivated mesa photodiodes do slightly better.

A second approach to eliminating sidewall leakage is to eliminate the sidewalls altogether by processing diodes with a diffusion doping process. In such a process, an n-i-i structure rather than an n-i-p structure is grown on an n-substrate, and rather than defining individual pixels by etching mesas, pixels are defined by the diffusion of a p-dopant only into selected areas on the wafer, creating n-i-p pixels in only those selected areas. Typically, in a diffusion-doped process, the narrower bandgap n-i-i homojunction is capped with a thick, wider bandgap semiconductor.

To lay the groundwork for a diffusion doping approach, we have compared the performance of a superlattice pin without a GaSb window layer (ia1460) to a superlattice pin with a thick n-GaSb window layer. Quite apart from planar processing motivations, window layers are sometimes introduced to block minority carriers from reaching the semiconductor surface. Such window blocking layers may have two beneficial effects: they can improve the reverse breakdown bias voltage; and they can increase the minority carrier lifetime by preventing fast nonradiative recombination that occurs at surfaces.[14] Long carrier lifetimes have the effect of reducing the diffusion current (e.g. see Eq. 1), and thus improving the R_0A of diffusion-limited devices.

Figures 9 and 10 show a side-by-side comparison of the room-temperature performance of the two structures. They show that there is no improvement of the device by the introduction of the window layer. The lack of improvement in device performance may be because window blocking layers tend to be most beneficial when introduced on the p-side of

the junction, where the minority carriers are the more mobile electrons. But Figs. 9 and 10 also show there is no significant degradation in the performance.

6. Conclusion

In conclusion, through quantitative analysis of low and room temperature J-V curves and the temperature dependence of the zero bias dynamic resistance—area product R_0A, we have mapped out what factors limit R_0A in different temperature and mesa size regimes. At low temperatures, the performance of our largest mesa photodiode R_0A's are strongly limited by a shallow trap-assisted tunneling process (x300). Plots of $1/R_0A$ versus perimeter-to-area ratio show that small mesa diodes are further limited by perimeter leakage by a factor of about 20. The largest mesas at room temperature are devices limited predominantly by diffusion processes. Small radii mesas at room temperature are further limited by perimeter leakage by a factor of about 100. Dielectric passivation of mesa diodes with SiN had little effect on reducing perimeter leakage. We laid the groundwork for elimination of sidewalls altogether by testing the effect of window layers on the junctions, a prerequisite for planar processing. An n-GaSb window layer on the n-side of the junction neither improved nor degraded detector performance.

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