

InP-based Single Photon Avalanche Diodes

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Abstract—We describe recent results for the performance and modeling of InP-based single photon avalanche diodes. At 1.55 μm , dark count probabilities $<2 \times 10^{-7} \text{ ns}^{-1}$ have been achieved at 220K for a photon detection efficiency of 15%.

From the perspective of performance, cost, and reliability, InP-based single photon avalanche diodes (SPADs) are the most promising detector technology for numerous photon counting applications ranging from optical fiber-based quantum cryptography to shortwave infrared 3-D flash lidar imaging. In this paper, we describe our progress in improving the performance of InP-based SPADs. We present characterization data demonstrating a very low dark count rate (DCR) of less than 200 Hz for a photon detection efficiency (PDE) of 15% at 220 K. We also illustrate the dependence of DCR on gate repetition rate and show that afterpulsing remains below 5×10^{-4} for repetition rates up to 5 MHz for a PDE of 15%. Finally, we describe detailed modeling with which we have quantified the dominant dark carrier generation mechanisms and obtained a more comprehensive understanding of SPAD behavior given changes in operating conditions such as temperature and applied bias.

Our basic SPAD design relies on the use of an InGaAs(P) absorption region lattice-matched to InP substrates, combined with an InP multiplication region in a canonical separate absorption and multiplication (SAM) region avalanche diode structure. A thorough description of the device structure can be found in Ref. [1]. SPADs are operated in “Geiger-mode” by gating the applied bias V above the breakdown voltage V_b by an excess bias V_{ex} (i.e., $V_{ex} = V - V_b$). In this operating mode, a single photoexcited carrier can give rise to a macroscopic avalanche of charge which is detectable in a purely digital fashion using an appropriate threshold detection circuit. After detection, the avalanche is quenched using an appropriate quenching circuit [2].

The most fundamental trade-off in SPAD performance occurs in attempting to maximize PDE while minimizing DCR. PDE is the probability of an incoming photon generating a photoexcited carrier that is successfully detected. DCR is the probability per second that a carrier created by any mechanism other than photoexcitation (i.e., a dark carrier) is detected. PDE is increased by applying a larger V_{ex} since the probability P_a of inducing a detectable avalanche is enhanced by the associated increase in internal electric field. However, any increase in P_a is accompanied by a proportional increase in DCR. Moreover, if DCR has significant contributions from field-dependent dark carrier excitation mechanisms, it will exhibit an even faster rise with increasing V_{ex} compared to the rise in PDE.

To the extent that dark carrier generation is mediated by defects, good epitaxial material quality is critical to achieving low DCR. Beyond the base material quality, precise control of the internal electric field through epitaxial layer design is essential for minimizing field-induced dark carriers. Through successive design iterations and comprehensive modeling (described below), we have made substantial improvements in the DCR vs. PDE trade-off.

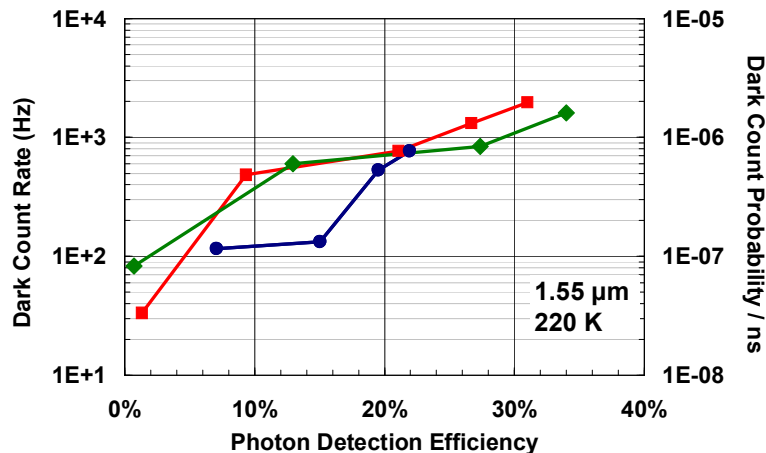


Fig. 1. Dependence of dark count rate and dark count probability per 1-ns gate on photon detection efficiency for three SPADs with a 25- μm optical diameter.

In Figure 1, we illustrate DCR vs. PDE data for three SPADs with a 25- μm optical diameter. Device-to-device performance variations exist due to local variations in material quality and epitaxial structure. The two devices for which data is indicated by squares and diamonds were taken from the same wafer. The data indicated by circles is from

a device from a more recent iteration in which the multiplication width was increased relative to previous iterations. This latter device achieves a DCR < 200 Hz for a 15% PDE at a temperature of 220 K, easily obtained using thermoelectric coolers.

Each data point in Figure 1 was obtained by measuring DCR and PDE at a fixed value of V_{ex} using short 1-ns gates with a repetition rate of 500 kHz [3]. The bias circuitry has a fixed voltage swing $\Delta V \sim 4$ V. Proper operation results when a dc bias $V_{dc} < V_b$ is used in conjunction with ΔV ; this imposes a limitation that V_{ex} must be less than ΔV . If V_{dc} exceeds V_b , then there will be a non-zero DCR even when the device is supposed to be in the quenched state. This results in a faster rise in DCR with increasing PDE. We see some evidence of this effect for the higher DCR data points in each of the curves in Figure 1. However, we have included these points to illustrate worst case DCR for PDE values on the order of 30%. Bias circuitry with larger ΔV would enable higher PDE values to be obtained.

Many single photon counting applications require counting rates well beyond 1 MHz. With SPADs, operation at faster repetition rates is hampered by a rate-dependent increase in the DCR. With each avalanche event, some fraction of the electrical carriers created will become trapped at defects in the multiplication region and will be thermally detrapped without consequence while the SPAD is in its quenched state. However, if a significant number of trapped carriers are still being detrapped when the gate is re-applied, then they can trigger a dark count and increase DCR. Shorter periods of time between gates will lead to a higher probability of dark counts induced by detrapped carriers. These dark counts which exceed the intrinsic (i.e., low repetition rate) DCR are generally referred to as "afterpulses."

In Figure 2, we present measurements of the probability of an afterpulse within a 1-ns gate as a function of PDE for a number of different repetition rates. For rates between 500 kHz and 5 MHz, the afterpulse probability (APP) at 15% PDE increases roughly proportionally with the repetition rate. At 5 MHz, the APP of $< 5 \times 10^{-4}$ at 15% PDE would generally be acceptable for many applications. However, for a 10 MHz rate, APP jumps dramatically—by nearly three orders of magnitude—for a PDE of 15%. This behavior indicates that for the operating conditions described, a detrapping time constant on the order of 0.1 μ s results in a drastic change in APP for a repetition rate increase from 5 MHz to 10 MHz.

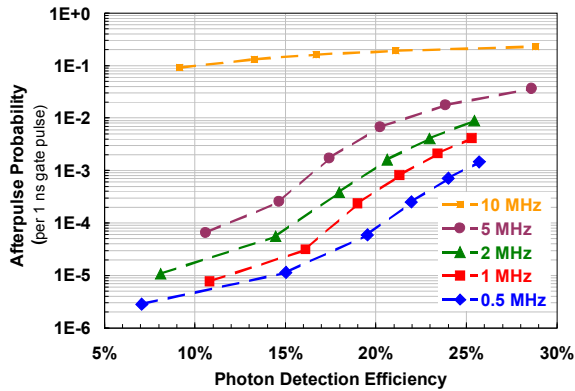


Fig. 2. Afterpulse probability vs. PDE as a function of repetition rate.

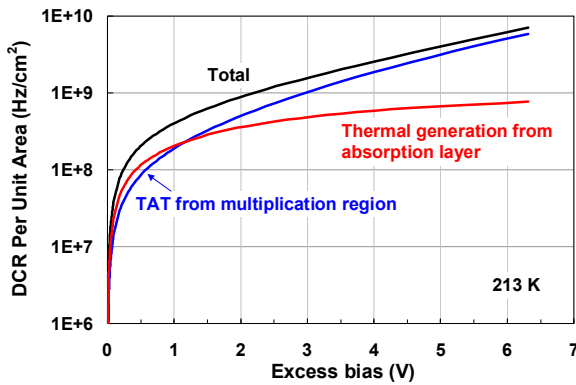


Fig. 3. Modeling results for dominant dark count rate contributions vs. excess bias for a 1.5 μ m SPAD.

To gain a more comprehensive understanding of various trade-offs in SPAD performance, we have carried out extensive device modeling. Following the formalism in Ref. [4], we have computed DCR vs. PDE with the goal of identifying the dominant leakage mechanisms so that device performance can be optimized for various operating conditions. In Figure 3, we present modeling results showing the calculated dependence of the dark count rate per unit area on excess bias V_{ex} . Among all layers in the structure, dark carrier generation is dominated by (i) trap-assisted tunneling (TAT) in the InP multiplication region and (ii) thermal generation in the InGaAs absorption region. At 213K, these two mechanisms have comparable contributions for V_{ex} up to ~ 2 V; for higher voltages, the TAT mechanism dominates. At somewhat higher temperatures (e.g., 240 K), thermal generation dominates for $V_{ex} < 5$ V. These model results have guided the optimization of SPAD design for different operating conditions such as temperature, bias, and alternative operating wavelengths (e.g., 1.06 μ m [5] and 1.3 μ m).

References

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